PCI EXPRESS: BEYOND MINIMUM COMPLIANCE

You'll need to go beyond the basics embodied in the PCI-SIG committee's software if you want to best your competitors in the PCI Express arena.

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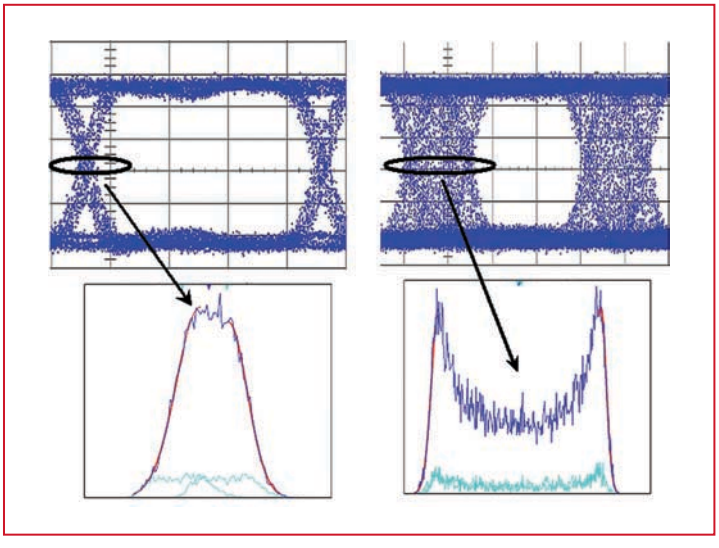
A compliance testing software package available for free download from the PCI-SIG committee is an excellent, simple tool for preliminary demonstration of a product's compliance to PCI Express 1.1 standards. Indeed, that package was the predominant tool used to demonstrate product compliance at a PCI Express plugfest held in San Jose, CA, December 5–9, 2005.



You should note, however, that this software was designed to provide a "snapshot" of minimum compliance and was never designed to be a complete compliance tool for PCI Express. The SIG software measures and reports on just four parameters (V_{TXA}, V_{TXA_d}, T_{TXA}, $T_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$), while the specification for full compliance requires manufacturers to measure and report on a total of 30 parameters, in accordance with the PCI Express, Revision 1.1 Base Specification and Card Electromechanical Specification (Refs. 1 and 2). **Tables 1** and **2** show differential transmitter output specifications and differential receiver input specifications, respectively. In addition, reference clock peak-to-peak phase jitter must not exceed 86 ps for a 10^{-6} BER or 108 ps for a 10^{-12} BER. (See "REFCLK phase jitter specifications" accompanying the online version of this article at www.tmworld.com/2006_08).

The PCI SIG software is useful for customer demonstrations, but more-robust commercial compliance-test packages, which are available from a va-

FIGURE 1. The top right eye diagram indicates degraded performance relative to that depicted in the top left diagram. The corresponding histograms suggest the lack of a PCI Express-compliant clock.

riety of vendors, address the comprehensive list of parameters called out by the PCI Express specifications. You can take advantage of these commercial packages to create products that are not just compliant, but that have higher design margins and improved production yields.

When evaluating commercial packages, you should compare their capabilities with respect to the PCI Express specifications to find the package that performs the tests you need. You should also take the time to understand the methods each package uses for the underlying measurements, as these measurements are used to derive other results during parametric (jitter, noise, and BER, also termed JNB) testing.

The best test methods, test instruments, and software packages to use are those that come closest to taking direct measurements for the parameters that apply to your products. You may need to use several instruments and methods—each one providing a "best method" for some portion of the list of parameters to be measured and reported on.

Using the right compliance tools is not a "nice to have" capability but a matter of maintaining competitiveness in the marketplace. Passing parts that have limited design margins can cause serious business issues. While such parts may pass the minimum compliance tests, if they later fail in the field, they will affect the bottom-line profits of a product line or business unit.

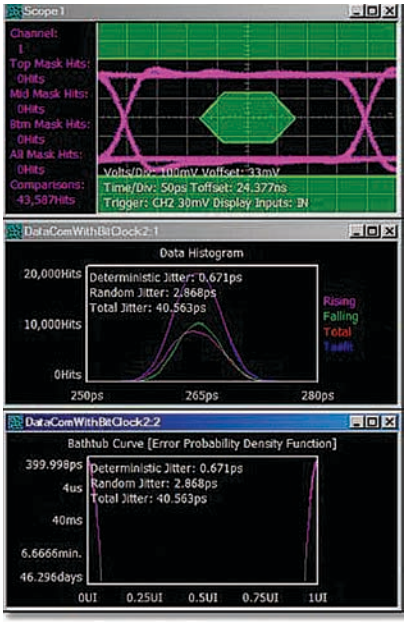


FIGURE 2. An eye mask (top) enables go/no-go testing, while a histogram (middle) indicates the jitter of rising and falling data edges relative to the clock signal. The bathtub curve data enables derivation of DJ, RJ, and TJ values using a tail-fit algorithm.

Table 1. Differential transmitter output specifications

SYMBOL	PARAMETER AND DEFINITION	1.1 SPEC
UI	Unit interval	399.88 ps (min) 400.12 ps (max)
$V_{TX-DIFFp-p}$	Differential peak-to-peak TX voltage swing	0.8 V (min) 1.2 V (max)
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (ratio)	–3.0 dB (min) –3.5 dB (nominal) –4.0 dB (max)
T_{TX-EYE}	Minimum transmitter eye width	0.75 UI (min)
$T_{TX-EYE-MEDIAN-TO-MAX\_JITTER}$	Maximum time between the jitter median and maximum deviation from the median	0.125 UI (max)
$T_{TX-RISE,\ TX-FALL}$	D+/D– TX output rise/fall time	0.125 UI (min)
$V_{TX-CM-ACp}$	RMS AC peak common-mode output voltage	20 mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common-mode voltage during l/O and electrical idle	0 mV (min) 100 mV (max)
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D–	0 mV (min) 25 mV (max)
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0 mV (min) 20 mV (max)
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection	600 mV (max)
$V_{TX-RCV-CM}$	TX DC common-mode voltage	0 V (min) 3.6 V (max)
$I_{TX-SHORT}$	TX short-circuit current limit	90 mA (max)

Table 2. Differential receiver input specifications

SYMBOL	PARAMETER AND DEFINITION	1.1 SPEC
UI	Unit interval	399.88 ps (min) 400.00 ps (nominal) 400.12 ps (max)
$V_{RX-DIFFp-p}$	Differential input peak-to-peak voltage	0.175 V (min) 1.2 V (max)
T_{RX-EYE}	Minimum receiver eye width	0.4 UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	150 mV (max)
$V_{RX-CM-ACp}$	AC peak common-mode voltage	0.4 UI (min)

Analyzing failures

You should also look for a PCI Express compliance tool that can perform failure analysis when a part fails on the production line or is returned from the field. Since compliance tools, by definition, are used to measure designs *after* they are complete, many packages provide limited or no diagnostic tools to aid a developer in isolating the root cause of the failed parameter. But if you use a tool that does offer failure analysis, you can quickly isolate the source of a problem and find a solution. Faster resolution of incidents results in improved customer satisfaction and overall better performance in the marketplace.

Robust packages provide diagnostic tools for both clock *and* data. Without first verifying the clock signal is accurate, you are at risk for propagating relatively small errors into very large errors.

Here are some examples of detailed views used for diagnostics. **Figure 1**

shows the test results of a PCI Express data signal with and without using a compliant clock. **Figure 2** shows an eye diagram, a jitter histogram, and bathtub measurements on a PRBS 2^{23}–1 pattern. The Wavecrest TailFit algorithm (Refs. 3 and 4) applied to the jitter histogram yields RJ, DJ, and TJ results in about 1 s, measuring a signal from a pattern generator.

Other functions that can help evaluate PCI Express compliance include marker tools that can indicate jitter characteristics in several formats, including fast Fourier transforms (FFTs). In addition, clock/PLL tools can help isolate the cause of a Serdes problem that stems from a faulty reference clock or PLL. The online version of this article shows graphical examples of marker and clock/PLL tools and illustrates, for example, how you can use FFT and 1-sigma vs. span views to identify sources of jitter such as crosstalk or power-supply noise in order to find and eliminate problems (www.tmworld.com/2006_08).

A final example demonstrates the importance of diagnostic tools. Consider the test results for a transmitter that has been tested for compliance to PCI Express. **Figure 3** depicts the transmitter signal/jitter output test results for the full-swing eye (Figure 3a), de-emphasis eye (Figure 3b), and BER cumulative distribution function (CDF) and associated TJ at BER = 10^{-12} (Figure 3c).

In this figure, the measured eye-opening is 0.694 UI (or TJ = 61.2 ps). The minimum specification for the transmitter eye opening is 0.75 UI; therefore, this PCI transmitter marginally fails the compliance test.

Figure 4 shows the data-dependent jitter (DDJ) distribution, PJ, and RJ power-spectrum density (PSD) for the same transmitter. Transmitter jitter output diagnostics test results measure DDJ as a function of the UI span. The DDJ histograms are reviewed for rising (green) and falling (purple) edges, respectively. The lower left diagram depicts a "zoom in" for the worst-case DDJ locations. The lower right diagram shows both PJ and RJ PSD shape.

These diagnostic views provide valuable information for determining the major jitter contribution. In this example, a PJ value at 5 MHz with a magnitude of 20.9 ps was the underlying problem. Had this PJ been identified and removed early in the development cycle, the transmitter would have passed the compliance test with high design margin. The DDJ in this case is 20.76 ps, and RJ rms is 1.4 ps, and both were determined to not be the major contributing factors.

Once you choose a software package for your PCI Express compliance tests, you should use the same instruments and test methodology throughout the entire product cycle. This will permit a seamless transition from development to design characterization to high-volume production, which will save time, reduce test costs, and improve time-to-market for your company. Using a single methodology in all cases will eliminate the confusion that could arise from measured values that were generated by different methods and platforms. T&MW

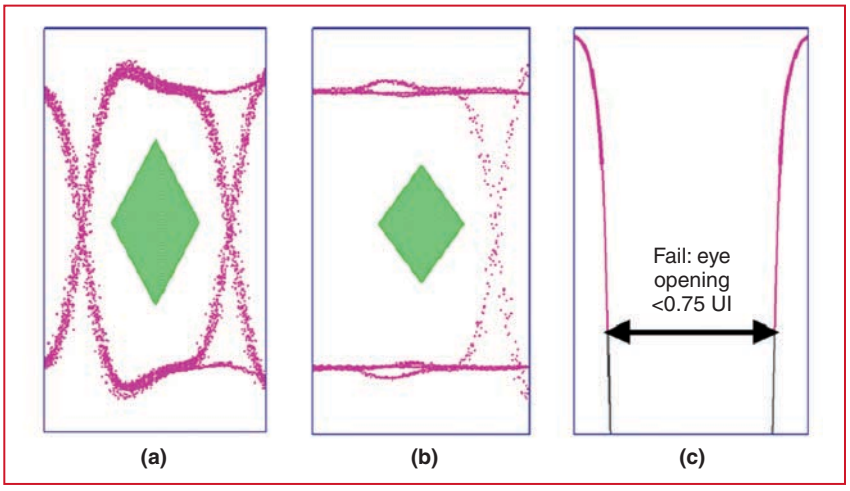


FIGURE 3. These images show the test results for a transmitter's signal/jitter output and associated TJ at BER = 10^{-12}: (a) full-swing eye, (b) de-emphasis eye, and (c) BER CDF bathtub curve.

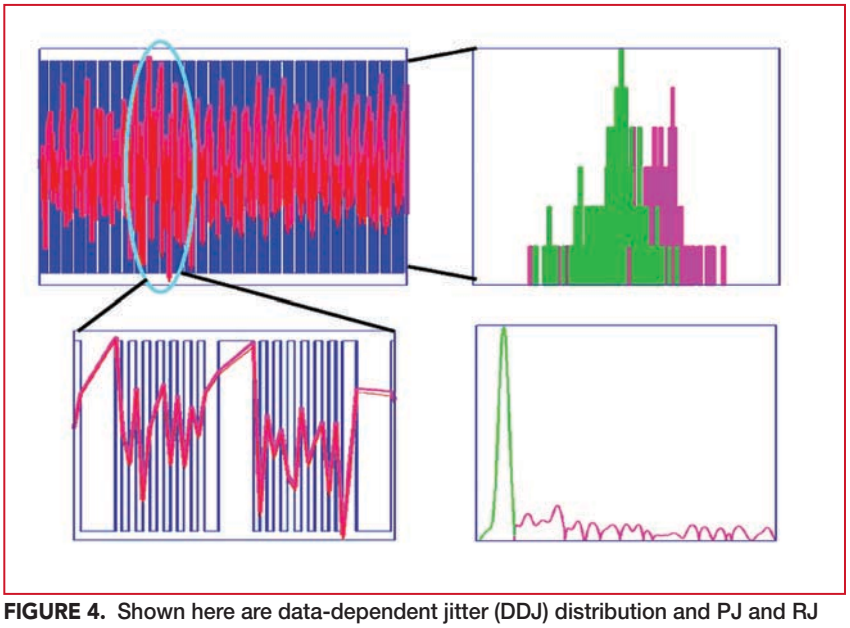


FIGURE 4. Shown here are data-dependent jitter (DDJ) distribution and PJ and RJ power-spectrum density (PSD) for the transmitter that failed the compliance test in Figure 3. The DDJ histograms are reviewed for rising (green) and falling (purple) edges, respectively. The lower left diagram depicts a "zoom in" for the worst-case DDJ locations, and the lower right graph shows both PJ and RJ PSD.

REFERENCES

1. "PCIe Base Specification 1.1," PCI SIG, 2005. www.pcisig.com/specifications/pciexpress/base.

2. "PCIe Card Electromechanical Specification 1.1," PCI SIG, 2005, www.pcisig.com/specifications/pciexpress/base.

3. "Signal-Integrity Analysis Tool Targets PCI Express and SATA II," Test & Measurement World Online, August 12, 2005, www.reed-electronics.com/tmworld/article/CA634594.

4. Nelson, Rick, "Serdes devices challenge ATE," *Test & Measurement World*, August 2002, www.tmworld.com/archives.

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Dr. Mike Li, *chief technology officer for Wavecrest, pioneered the tail-fit jitter separation method and has been involved in setting standards for jitter, noise, and signal integrity for serial data communication. He has more than 15 years experience in high-speed instrumentation for both electrical and optical communication. He has a BS in physics from University of Science and Technology of China, and he has an MSE in electrical engineering and a PhD in physics from the University of Alabama in Huntsville. He has done post-doctorate work at the University of California, Berkeley. Dr Li has published more than 70 papers and has filed nine patents, with two granted and seven pending.*

Rich Vignes, *director of marketing for Wavecrest, has 20 years experience in business development, product marketing, and product management. He has formed numerous strategic partnerships and alliances to facilitate bringing whole solutions to the market. He has a BSME degree from the University of Minnesota and has two patents pending.*

ON THE WEB

Various tools can help you evaluate a product's compliance to PCI Express. The online version of this article shows graphical examples of marker and clock/PLL tools and illustrates how you can use FFT and 1-sigma vs. span views to identify sources of jitter such as crosstalk and power-supply noise. **www.tmworld.com/2006_08.**